Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **OUTPUT A**
2. **– INPUT A**
3. **+ INPUT A**
4. **GND**
5. **+ INPUT B**
6. **– INPUT B**
7. **OUTPUT B**
8. **V +**

**.037”**

**.048”**

**7 8 1**

**2 3 4 5 6**

**L**

**M**

**1**

**5**

**8**

**D**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .0036” X .0036”**

**Backside Potential: GND**

**Mask Ref: LM158D**

**APPROVED BY:DK DIE SIZE .037” X .048” DATE: 3/8/23**

**MFG: NATIONAL SEMI THICKNESS: .013” P/N: LM158 MD8**

**DG 10.1.2**

#### Rev B, 7/19/02